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Buck-boost-flyback integrated converter with single switch to achieve high voltage gain for PV or fuel-cell applications

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Abstract: This study presents a buck-boost-flyback integrated converter (BBFIC), which can step up the voltage of photovoltaic (PV) module or fuel cell to a much higher level for grid-tied applications. The converter combines two buck-boost converters and one flyback converter into a single-stage structure with single power switch. In the power stage, an inductor and a coupled inductor are adopted to feature buck-boost and flyback behaviours, and three capacitors are connected in series to stack up output voltage. Even though it possesses the characteristics of buck-boost and flyback converters, the problem of reversed voltage polarity is avoided and the energy stored in leakage inductor can be recycled without additional active clamp circuits. The structure of BBFIC can be easily expanded to obtain an extra-high voltage gain by stacking buck-boost cells or flyback cells. Voltage gain derivation and theoretical analysis are detailed in this study. Simulations and practical results measured from a prototype have validated the proposed BBFIC.

1 Introduction

Recently, green power systems, such as photovoltaic (PV) module and fuel cells, attract a great deal of attentions, which have been widely used in industry and residential areas for air pollution reduction. However, low terminal voltage is their common shortcoming [1–3]. For grid-tied applications, the dc input voltage of an inverter has to be high enough to inject power into utility [4, 5]. Accordingly, a frond-end dc/dc converter with high voltage gain is required to step up the terminal voltage of PV module or fuel cells. Traditional boost converter and isolated converters theoretically can achieve high voltage gain by means of heavy-duty operation or high turns ratio, but in practice, converter efficiency is degraded dramatically. To overcome this problem, high voltage gain dc/dc converter is developed.

Generally, a high voltage gain dc/dc converter adopts switched capacitors and/or coupled inductors to obtain high output voltage [6–10]. While incorporating coupled inductor, a converter will processes flyback and/or forward behaviours [11–13]. That is, additional active clamp circuits are required to recycle leakage energy and lower voltage stress of semiconductor device but this approach increases cost. Literature [14, 15] presents two high step-up converters but both of them employ four active switches for voltage clamping and current controlling to achieve high voltage gain. Adopting a large number of power switches disadvantages industrial applications. Besides, for achieving much higher voltage gain, heavy-duty ratio and high turns ratio will be their only solutions, which still encounter the problem of low conversion efficiency. In [16, 17], the converters are able to accomplish extra-high voltage gain by stacking voltage multiplier cells instead of operating in heavy duty ratio or high turns ratio but voltage multiplier cell includes active switch. More power switches have to be used, which increases cost and control complexity significantly. Some converters complete high step-up voltage feature by means of cascading power stages [18, 19], which really can obtain a high level of output voltage with uncomplicated control scheme but overall efficiency will be another issue. In [20], a preliminary topology of the high voltage-gain converter is figured out; however, it lacks for comprehensive analysis, theoretical derivation, and detailed practical measurements.

This paper proposes a buck-boost-flyback integrated converter (BBFIC), which not only can achieve high voltage gain but has the feature of stacking expansion to accomplish an extra-high output voltage even if only one power switch is used. The BBFIC integrates two buck-boost converters and one flyback converter into single-stage structure, as shown in Fig. 1. Since the proposed converter only adopts one active switch, it has the merits of simple power-stage configuration and easy control circuit design. In addition, the energy stored in leakage-inductor of coupled inductor can be totally recycled without additional active clamper or snubber circuit. An extra-high voltage gain can be easily carried out by stacking buck-boost cells or flyback cells.

This paper is organised as follows. Following the introduction, the operation principle of proposed BBFIC are described in Section 2, while the circuit performance and components design are analysed in Section 3. Section 4 focuses on the conduction loss derivation for efficiency estimation. Practically measured waveforms from a 200 W prototype are shown in Section 5 to demonstrate the feasibility and correctness of the BBFIC. Finally, the conclusion is summarised in Section 6.

2 Converter structure and operation principle

2.1 Converter structure

The equivalent circuit of the proposed BBFIC is shown in Fig. 2*a*, in which L_{BB} expresses the power choke of the buck-boost 1, L_m denotes the magnetising-inductor of the coupled inductor, L_{lk1} and L_{lk2} stand for the primary and secondary leakage inductors, respectively, *SW* is the common switch, and C_{ds} is the output capacitor of *SW*. If the currents flowing through L_m and L_{BB} are continuous, the operation of the converter can be divided into five modes over one switching cycle. In addition, the proposed converter can achieve a much higher voltage gain by stacking buck-boost cells or flyback cells. An illustration to depict the expanded structure with buck-boost stacking is shown in Fig. 2*b*, in which it can be found that only an active switch is used and this expansion is unsophisticated.

2.2 Operation principle

The equivalents associated with the five operation modes are illustrated in Figs. 3*a*–*e*. In addition, Fig. 4 depicts the

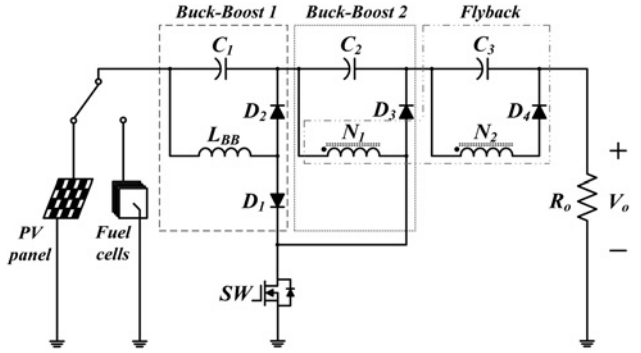

Fig. 1 *Power stage of the proposed BBFIC*

corresponding key waveforms. Analysis of the proposed converter begins by making these assumptions:

- Except the output capacitor of *SW*, all parasitic capacitors and internal resistors are neglected.
- All diodes are ideal.
- All capacitors are infinite so that the voltages across them are time-invariant.
- The magnetising-inductor L_m is much larger than the leakage-inductors L_{lk1} and L_{lk2}.
- The switching period is T_s. The common switch is closed for time DT_s and open for $(1-D)T_s$.

The operation principle of BBFIC is discussed mode by mode as follows:

2.2.1 Mode 1 [t_0, t_1]: This mode begins at time $t=t_0$. The equivalent circuit is referred to Fig. 3*a*. During this time interval, the status of the power switch *SW*is closed. Diodes D_2, D_3 and D_4 are reversely biased but D_1 is forward biased. Input voltage V_{in} is across inductor L_{BB} directly, and thus the current flowing through L_{BB} will increase linearly. At the same time, capacitor C_1 and input voltage will supply energy to L_m and L_{lk1}, which leads to a linear increase on the current flowing through L_m and L_{lk1}. The energy demand of load is powered by C_1, C_2, C_3 and V_{in}. This mode will end when the power switch *SW* is turned off, and then the operation of the converter will enter into Mode 2.

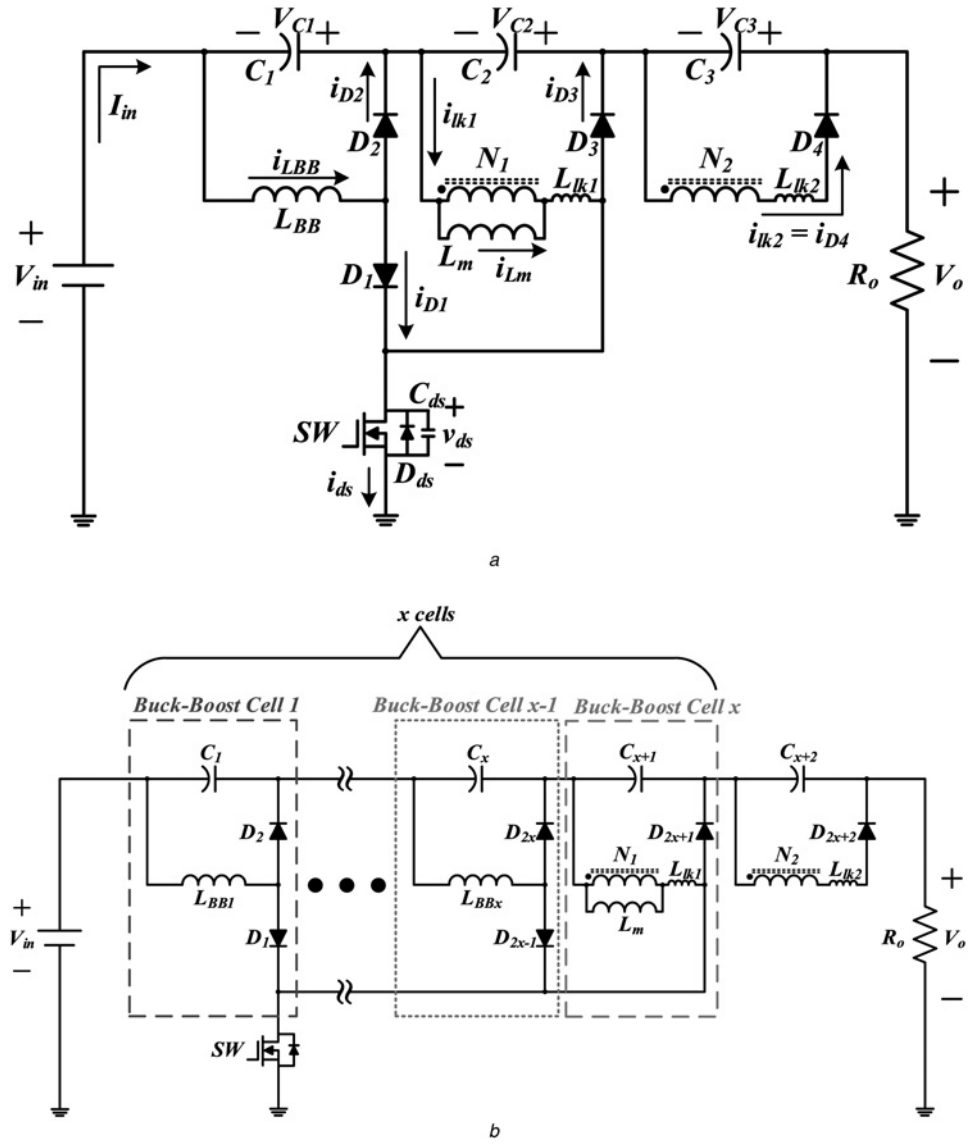

Fig. 2 *Converter equivalent*

a Equivalent circuit with the definitions of voltage polarity and current direction
b Illustration of structure expansion by stacking buck-boost cells for extra-high voltage gain achievement

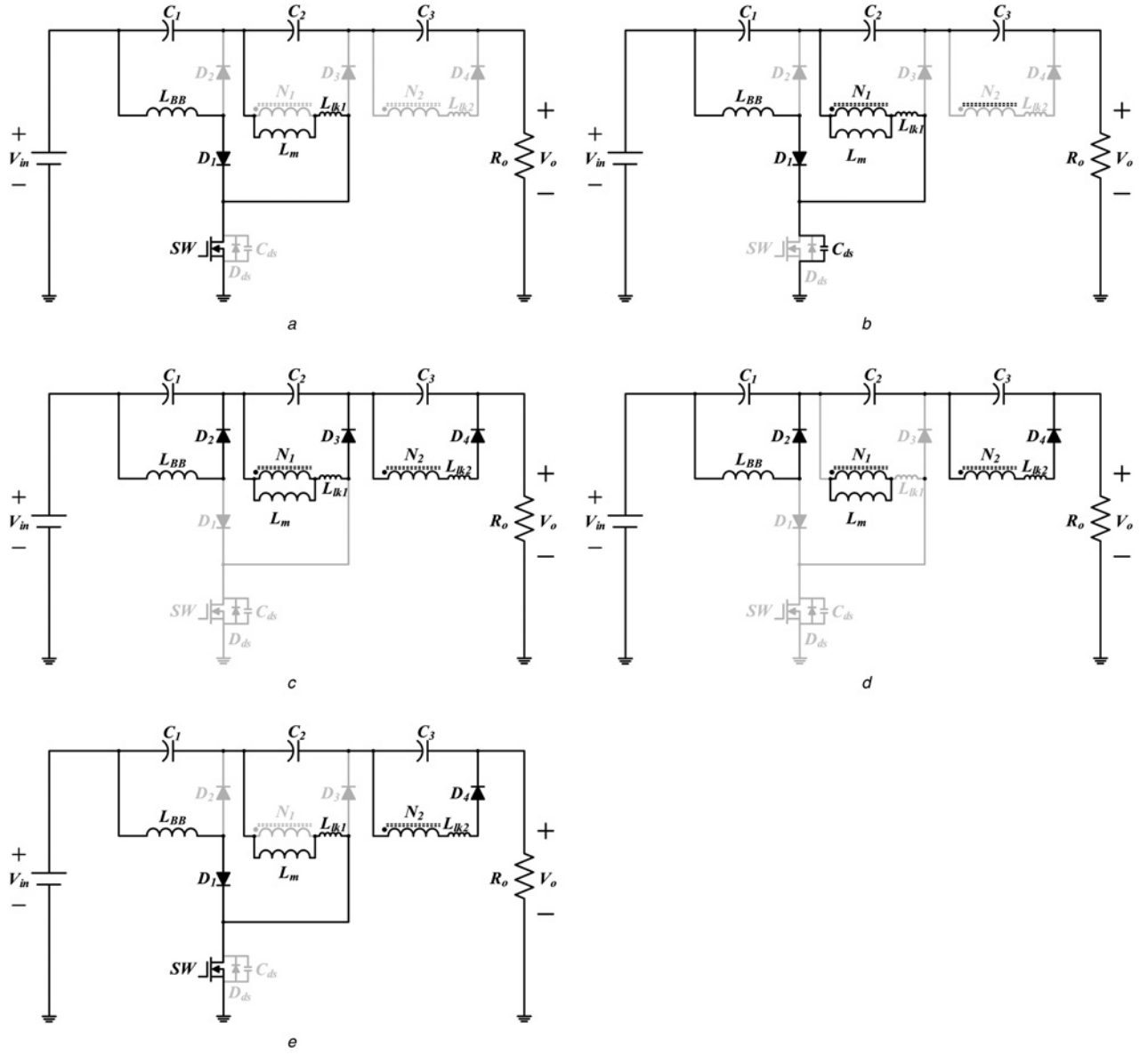

Fig. 3 *Equivalent circuits to illustrate the operation of the proposed converter*

a Mode 1
b Mode 2
c Mode 3
d Mode 4
e Mode 5

2.2.2 Mode 2 [t_1, t_2]: In Mode 2, diode D_1 is forward biased, whereas diodes D_2, D_3, and D_4 are reversely biased. The voltage polarities of inductors L_{BB} and L_{lk1} change instantaneously, and the voltage of parasitic-capacitor C_{ds} increases rapidly. Once the voltage across C_{ds} reaches $V_{in}+V_{C_1}+V_{C_2}$, the operation of the converter enters into next mode. The corresponding equivalent is shown in Fig. 3*b*.

2.2.3 Mode 3 [t_2, t_3]: During this time interval, *SW* is open and all diodes except D_1 are forward biased. The energy stored in L_{BB} is dumped to C_1 through diode D_2. Meanwhile, magnetising-inductor L_m provides energy to C_2 and C_3 via D_3 and coupled inductor, respectively. Since the energy stored in L_{lk1} is forwarded to C_2, the voltage across L_m and L_{lk1} will be equal to V_{C_2} and the current i_{lk1} decreases. Once i_{lk1}drops to zero, this mode ends. The corresponding equivalent is depicted in Fig. 3*c*.

2.2.4 Mode 4 [t_3, t_4]: Fig. 3*d* illustrates the equivalent of mode 4, in which common switch *SW* remains open. Diodes D_2 and D_4 are forward biased but D_1 and D_3 are off. Inductors L_{BB} and L_m keep on releasing energy to C_1 and C_3, respectively. This mode stops at the time that *SW* is turned on again.

2.2.5 Mode 5 [t_4, t_5]: At time $t=t_4$, *SW* is turned on and Mode 5 starts. The equivalent is shown in Fig. 3*e*. In this mode, the current i_{lk1} is built by V_{in} and V_{C_1}. Inductor L_{BB} absorbs energy from input V_{in}, and the $i_{L_{BB}}$ current increases. Meanwhile, the energy of L_{lk2} is recycled to C_3 via D_4. This mode will end when the current i_{D_4} decreases to zero, and then, the operation of the converter returns to Mode 1.

3 Circuit performance analysis and component design

This section will discuss the circuit performance, semiconductor device stress, and inductor design. Suppose that the converter operates in continuous conduction mode (CCM). In order to

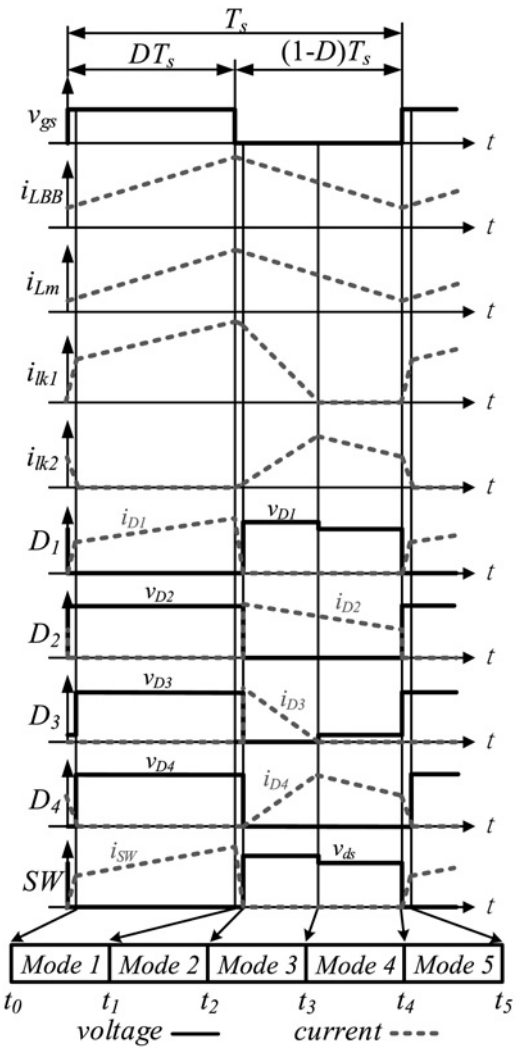

Fig. 4 *Conceptual key waveforms of the proposed converter over one switching cycle*

simplify mathematical derivation, leakage inductances L_{lk1} and L_{lk2} are both neglected because they are far less than magnetising inductance L_m. In addition, some assumptions are made as follows:

- The voltages across the capacitors, C_1, C_2, and C_3, are kept at constant.
- Active switch and all diodes are ideal.
- The turns ratio of secondary winding N_2 to primary winding N_1 is n.

3.1 Voltage-gain derivation

From the outermost loop in Fig. 2*a*, one can find that the output voltage equals V_{in} plus V_{C_1}, V_{C_2} and V_{C_3}. That is

$$V_{in} + V_{C_1} + V_{C_2} + V_{C_3} = V_o. \tag{1}$$

Equation (1) implies that the voltage gain of the converter (V_o/V_{in}) can be obtained after determining the relationships of V_{C_1}, V_{C_2} and V_{C_3} in terms of V_{in}.

Applying voltage-second balance criterion (VSBC) to the buck-boost 1 results in

$$V_{C_1} = \frac{D}{(1-D)} V_{in}. \tag{2}$$

For buck-boost 2, the voltage across L_m equals $V_{in} + V_{C_1}$ as switch on and is V_{C_2} as switch off. Similarly, based on VSBC and from (2), an expression for V_{C_2} is found as

$$V_{C_2} = \frac{D}{(1-D)^2} V_{in}. \tag{3}$$

The energy stored in the coupled inductor is also released to capacitor C_3 when switch is turned off. Supposed that the coupling coefficient of the coupled inductor is unity, the voltage across L_m will be equal to V_{C_3}/n. Then, applying VSBC to L_m and deriving with (2) can yield

$$V_{C_3} = \frac{nD}{(1-D)^2} V_{in}. \tag{4}$$

By substituting (2)–(4) into (1), the voltage gain of the proposed converter can be readily obtained

$$\frac{V_o}{V_{in}} = 1 + \frac{D}{1-D} + \frac{D}{(1-D)^2} + \frac{nD}{(1-D)^2} = \frac{1+nD}{(1-D)^2}. \tag{5}$$

If the BBFIC incorporates x buck-boost cells, as shown in Fig. 2*b*, its

Table 1 Performance comparison among the proposed and other high step-up converters

	[21]	[22]	[23]	[24]	Proposed
voltage gain	$(1+n)/(1-D)$	$(1+n+nD)/(1-D)$	$(1+n)/(1-D)$	$(1+n+nD)/(1-D)$	$(1+nD)/(1-D)^2$
number of MOSFETs	1	1	1	1	1
number of power diodes	3	5	3	4	4
number of capacitors	3	5	4	4	3
number of transformers	1	1	1	1	1
number of inductors	0	0	1	0	1
voltage stress of active switch	$V_o/(1+n)$	$V_o/(1+n+nD)$	$V_o/(1+n)$	$V_o/(1+n+nD)$	$V_o/(1+nD)$
maximum voltage stress among all power diodes	V_o	$nV_o/(1+n+nD)$	$nV_o/(1+n)$	$nV_o/(1+n+nD)$	$nV_o/(1+nD)$

Table 2 Performance comparison among the proposed and other multi-layer converters

	[18]	[25]	[26]	Proposed
voltage gain under x layers	$1/(1-D)^x$	$(2x+1+D)/(1-D)$	$x/(1-D)$	$1 + D/(1-D) + \cdots D/(1-D)^x + nD/(1-D)^x$
number of MOSFETs	x	1	$2x$	1
number of capacitors	x	$x+3$	$x+1$	$x+1$
number of power diodes	x	$2x+3$	0	$2x$

voltage gain can be determined by

$$\frac{V_o}{V_{in}} = 1 + \frac{D}{1-D} + \cdots \frac{D}{(1-D)^x} + \frac{nD}{(1-D)^x}. \quad (6)$$

Comparison between the proposed converter and other high step-up converters [21–24] is summarised in Table 1, from which it can be observed that the proposed converter is much more attractive than other similar converter in voltage gain. Regarding expanded structure, the multi-layer high step-up converters in [18, 25, 26] are considered. Table 2 summarises the performance comparison, which reveals that the BBFIC is still excellent in voltage gain.

3.2 Voltage stress of power semiconductor device

The determination of voltage stress of power semiconductor begins at the active switch *SW*. While the switch is open, from Fig. 3*c*, the blocking voltage of *SW*, $V_{SW,stress}$, can be estimated by

$$V_{SW,stress} = V_{in} + V_{C_1} + V_{C_2}. \quad (7)$$

Substituting (2) and (3) into (7) becomes

$$V_{SW,stress} = \frac{1}{(1-D)^2} V_{in}. \quad (8)$$

The voltage stress across diode D_1, $V_{D_1,stress}$, can also be determined as active switch is open, which is equal to V_{C_2}. That is

$$V_{D_1,stress} = \frac{D}{(1-D)^2} V_{in}. \quad (9)$$

As opposed to the determination of $V_{D_1,stress}$ in switch-off period, the voltage stresses across D_2, D_3 and D_4, denoted as $V_{D_2,stress}$, $V_{D_3,stress}$ and $V_{D_4,stress}$, are all determined in switch-on period. While switch is closed, the magnitude of $V_{D_2,stress}$ equals V_{in} plus V_{C_1}. From (3), the following expression holds

$$V_{D_2,stress} = \frac{1}{1-D} V_{in}. \quad (10)$$

Meanwhile, the series voltage of V_{in}, V_{C_1} and V_{C_2} will impose on D_3. That is

$$V_{D_3,stress} = V_{in} + V_{C_1} + V_{C_2}. \quad (11)$$

Substituting (2) and (3) into (11) results in

$$V_{D_3,stress} = \frac{1}{(1-D)^2} V_{in}. \quad (12)$$

With respect to $V_{D_4,stress}$, since the voltage across L_m is $V_{in} + V_{C_1}$, a blocking voltage on diode D_4 will be

$$V_{D_4,stress} = n\left(V_{in} + V_{C_1}\right) + V_{C_3}. \quad (13)$$

Rearranging (13) with (2) and (4), the following relationship can be obtained

$$V_{D_4,stress} = \frac{n}{(1-D)^2} V_{in}. \quad (14)$$

From (9), (10), (12), and (14), it can be found that if turns ratio n is greater than one, the diode D_4 will withstand a voltage higher than those across D_3, D_2 and D_1.

3.3 Current stress of power semiconductor device

Assume that the output load is a resistance of R_o. During the period of *SW* on, the capacitor C_3 discharges energy to the load and the magnitude of discharging current equals V_o/R_o. On the contrary, while *SW* off, C_3 charges and the charging current is $I_{D_4} - V_o/R_o$. Applying amp-second balance criterion (ASBC) to capacitor C_3 over one switching cycle can obtain

$$I_{D_4} = \frac{V_o}{(1-D)R_o}, \quad (15)$$

where I_{D_4} is the average current of D_4. With similar procedure to capacitor C_2, it can be found that the average current flowing through D_3 is identical to I_{D_4}. In order to obtain the peak current of D_3 and D_4, represented as $i_{D_3,peak}$ and $i_{D_4,peak}$, respectively, the average current of L_m, I_{L_m}, should be computed in advance. Because L_m dumps energy to C_2 and C_3 via D_3 and D_4, in turn, during the period of *SW* off, the magnitude of I_{L_m} will be the sum of I_{D_3} and nI_{D_4}. As a result, I_{L_m} can be represented as

$$I_{L_m} = \frac{V_o}{(1-D)R_o} + \frac{nV_o}{(1-D)R_o} = \frac{(1+n)V_o}{(1-D)R_o}. \quad (16)$$

After I_{L_m} is given, the peak current of D_3 and D_4 can be estimated as follows

$$i_{D_3,peak} = i_{D_4,peak} = \frac{1}{1+n}\left(I_{L_m} + \frac{1}{2}\int_{t_0}^{t_0+DT_s} \frac{V_{in} + V_{C_1}}{L_m}\,dt\right). \quad (17)$$

To find the current stress of D_2, the ASBC has to be applied to capacitor C_1. Capacitor C_1 dumps energy to L_m and R_o while *SW* on, and absorbs energy from L_{BB} via D_2 while *SW* off. That is

$$\left(-\frac{V_o}{R_o} - I_{L_m}\right)DT_s + \left(I_{D_2} - \frac{V_o}{R_o}\right)(1-D)\cdot T_s = 0, \quad (18)$$

where I_{D_2} stands for the average current of diode D_2. Rearranging (18) yields

$$I_{D_2} = \frac{(1+nD)V_o}{(1-D)^2 R_o}. \quad (19)$$

As discussed in Section 2, diode D_1 carries a current of $i_{L_{BB}}$ when *SW* is closed. In addition, the current flowing through D_2 is also $i_{L_{BB}}$ when *SW* is open. Therefore, the average currents of L_{BB} and D_1 are identical to I_{D_2}. That is, $I_{L_{BB}} = I_{D_1} = I_{D_2}$. Consequently, the peak currents of D_1 and D_2, $i_{D_1,peak}$ and $i_{D_2,peak}$, can be determined by

$$i_{D_1,peak} = i_{D_2,peak} = I_{L_{BB}} + \frac{1}{2}\int_{t_0}^{t_0+DT_s} \frac{V_{in}}{L_{BB}}\,dt. \quad (20)$$

The voltage source supplies energy to L_{BB} and L_m as *SW* in on-state hence the average current flowing through *SW* is the sum of $I_{L_{BB}}$ and I_{L_m}, which is expressed as

$$I_{SW} = I_{L_{BB}} + I_{L_m} = \frac{(2-D+n)V_o}{(1-D)^2 R_o}. \quad (21)$$

Once the average switch current I_{SW} is obtained, the switch peak

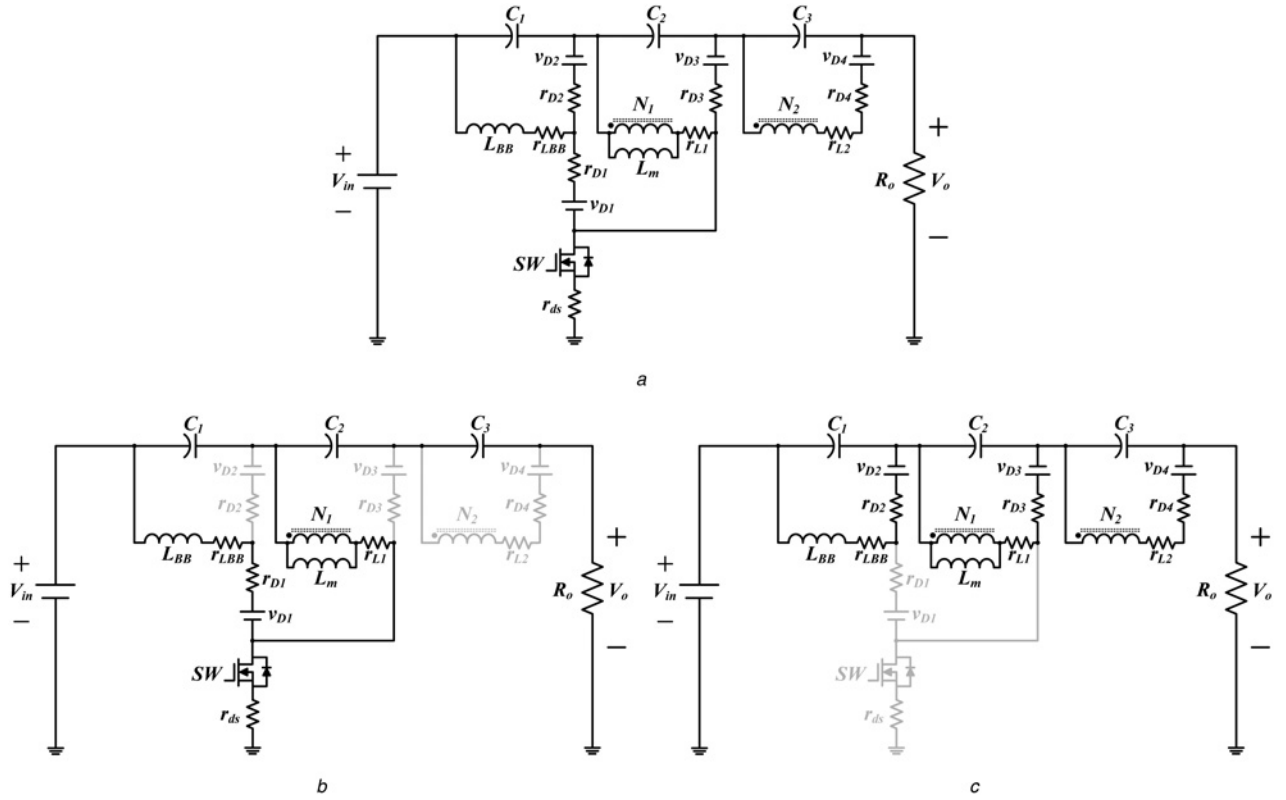

Fig. 5 *Equivalent of BBFIC with non-ideal components*

a Equivalent circuit for conduction loss calculation
b Equivalent circuit when SW is turned on
c Equivalent circuit when SW is turned off

current, $i_{\mathrm{SW,peak}}$, can be estimated by the following relationship:

$$i_{\mathrm{SW,peak}} = I_{\mathrm{SW}} + \frac{1}{2}\int_{t_0}^{t_0+DT_{\mathrm{s}}} \frac{V_{\mathrm{in}}}{L_{\mathrm{BB}}}\,\mathrm{d}t + \frac{1}{2}\int_{t_0}^{t_0+DT_{\mathrm{s}}} \frac{V_{\mathrm{in}}+V_{C_1}}{L_{\mathrm{m}}}\,\mathrm{d}t. \quad (22)$$

3.4 Design for inductances

The followings will deal with the inductance design of L_{BB} and L_{m}. When the proposed converter operates in CCM and steady state, the minimum values of magnetising current can be expressed as

$$I_{L_{\mathrm{m(min)}}} = I_{L_{\mathrm{m}}} - \frac{\Delta i_{L_{\mathrm{m}}}}{2}, \quad (23)$$

in which the change in magnetising current, $\Delta i_{L_{\mathrm{m}}}$, can be estimated by

$$\Delta i_{L_{\mathrm{m}}} = \frac{\left(V_{\mathrm{in}}+V_{C_1}\right)DT_{\mathrm{s}}}{L_{\mathrm{m}}}. \quad (24)$$

To determine the boundary between continuous and discontinuous current, the minimum current $I_{L_{\mathrm{m(min)}}}$ is set to zero. Then, substituting (16) and (24) into (23) yields

$$\frac{(1+n)V_{\mathrm{o}}}{(1-D)R_{\mathrm{o}}} - \frac{(V_{\mathrm{in}}+V_{C_1})}{2L_{\mathrm{m}}}DT_{\mathrm{s}} = 0. \quad (25)$$

From (2), (5), and (25), solving for minimum value of L_{m} for continuous current operation results in

$$L_{\mathrm{m(min)}} = \frac{D\cdot(1-D)^3R_{\mathrm{o}}}{2\cdot(1+n)\cdot(1+nD)\cdot f_{\mathrm{s}}}. \quad (26)$$

If inductance of L_{m} is less than $L_{\mathrm{m(min)}}$, the current $i_{L_{\mathrm{m}}}$ will be in discontinuous pattern. As a result, the voltages across C_2 and C_3 increase. That is, semiconductor devices, D_1, D_3, D_4, and SW, will endure a higher level of voltage stress. Since capacitor C_1 is only charged by L_{BB}, the magnitudes of capacitor voltage V_{C_1} and the blocking voltage $V_{D_2,\mathrm{stress}}$ are uninfluenced by the discontinuousness of $i_{L_{\mathrm{m}}}$.

Regarding the determination of the minimum inductance of L_{BB} in CCM, it starts with $I_{L_{\mathrm{BB(min)}}}$ as follows

$$I_{L_{\mathrm{BB(min)}}} = I_{L_{\mathrm{BB}}} - \frac{\Delta i_{L_{\mathrm{BB}}}}{2}, \quad (27)$$

where $I_{L_{\mathrm{BB}}}$ is equal to I_{D_2} calculated by (19). In addition, the current change on L_{BB}, $\Delta i_{L_{\mathrm{m}}}$, can be estimated by

$$\Delta i_{L_{\mathrm{BB}}} = \frac{V_{\mathrm{in}}DT_{\mathrm{s}}}{L_{\mathrm{BB}}}. \quad (28)$$

Then, let $I_{L_{\mathrm{BB(min)}}}$ equal zero. Rewriting (27) results in

$$\frac{(1+nD)V_{\mathrm{o}}}{(1-D)^2R_{\mathrm{o}}} - \frac{V_{\mathrm{in}}}{2L_{\mathrm{BB}}}DT_{\mathrm{s}} = 0. \quad (29)$$

Using (5) and solving for L_{BB}, the minimum inductance of the choke

in buck-boost 1 for CCM operation can be readily found as

$$L_{\mathrm{BB(min)}} = \frac{D(1-D)^3 R_{\mathrm{o}}}{2(1+nD)^2 f_{\mathrm{s}}}. \tag{30}$$

If L_{BB} is low enough to operate in discontinuous conduction mode (DCM), no matter what L_{m} operates in CCM or DCM, the voltages of all capacitors, C_1, C_2, and C_3, will increase. Hence, all semiconductor devices, D_1, D_2, D_3, D_4, and SW, have to encounter higher voltage stresses.

4 Analysis of converter efficiency

When a converter operates in CCM, converter loss will dominate conversion efficiency. In this section, the estimation of conduction loss is discussed under the consideration of winding resistance, diode forward voltage, and the on-state resistances of diode and switch. Fig. 5*a* shows the equivalent circuit for conduction loss computation, in which $r_{L\mathrm{BB}}$ stands for the resistance of L_{BB}, r_{ds} is the on-state resistance of the active switch, r_{L_1} and r_{L_2} denote the resistance of the primary winding and secondary winding of coupled inductor, respectively, and v_{D_1} , v_{D_2}, v_{D_3}, and v_{D_4} are the forward voltages of D_1, D_2, D_3 and D_4, in turn. Since leakage inductance is far smaller than magnetising inductance, the narrow time interval accompanied with leakage-energy releasing can be neglected.

Fig. 5*b* illustrates the equivalent circuit when switch is closed. Applying Kirchhoff's voltage law (KVL) to the closed loops of $V_{\mathrm{in}} - L_{\mathrm{BB}} - D_1 - SW$ and $V_{\mathrm{in}} - C_1 - N_1 - SW$ follows that

$$V_{\mathrm{in}} - v_{L_{\mathrm{BB}}} - i_{L_{\mathrm{BB}}}\left(r_{L_{\mathrm{BB}}} + r_{D_1}\right) - v_{D_1} - \left(i_{L_{\mathrm{BB}}} + i_{L_{\mathrm{m}}}\right) r_{ds} = 0 \tag{31}$$

and

$$V_{\mathrm{in}} + V_{C_1} - v_{L_{\mathrm{m}}} - i_{L_{\mathrm{m}}} r_{L_1} - \left(i_{L_{\mathrm{m}}} + i_{L_{\mathrm{BB}}}\right) r_{ds} = 0, \tag{32}$$

respectively. When SW is turned off, the corresponding equivalent circuit is depicted in Fig. 5*c*. By applying KVL to the loops of $L_{\mathrm{BB}} - D_2 - C_1$, $N_1 - D_3 - C_2$, and $N_2 - D_4 - C_3$, the following relationships hold

$$v_{L_{\mathrm{BB}}} + i_{L_{\mathrm{BB}}}\left(r_{L_{\mathrm{BB}}} + r_{D_2}\right) + v_{D_2} + V_{C_1} = 0, \tag{33}$$

$$v_{L_{\mathrm{m}}} + i_{D_3}\left(r_{L_1} + r_{D_3}\right) + v_{D_3} + V_{C_2} = 0, \tag{34}$$

and

$$n v_{L_{\mathrm{m}}} + i_{D_4}\left(r_{L_2} + r_{D_4}\right) - v_{D_4} - V_{C_3} = 0. \tag{35}$$

Equations (31)–(35) are useful to the derivation of the converter efficiency.

The efficiency of a converter is calculated by

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{o}} + P_{\mathrm{loss}}} = \frac{(V_{\mathrm{o}})^2/R_{\mathrm{o}}}{((V_{\mathrm{o}})^2/R_{\mathrm{o}}) + P_{\mathrm{loss}}}, \tag{36}$$

which reveals that for efficiency evaluation, output voltage V_{o} and power loss P_{loss} have to be determined in advance. Finding for V_{o} will be dealt with first. In BBFIC, V_{o} is the sum of V_{in}, V_{C_1}, V_{C_2} and V_{C_3}, as expressed in (1). The followings will determine V_{C_1}, V_{C_2} and V_{C_3} in the consideration of parasitic parameters. Assume that L_{m} and L_{BB} are large enough to keep the $i_{L_{\mathrm{m}}}$ and $i_{L_{\mathrm{BB}}}$ at constant. By applying VSBC to L_{BB} and deriving with (31) and (33), the voltage across C_1, while the converter counts for the effect of parasitic resistances and diode forward voltages, can be found as

$$\begin{aligned}&\left(V_{\mathrm{in}} - I_{L_{\mathrm{BB}}}\left(r_{L_{\mathrm{BB}}} + r_{D_1}\right) - v_{D_1} - \left(I_{L_{\mathrm{BB}}} + I_{L_{\mathrm{m}}}\right) r_{ds}\right)\\ &\times \frac{D}{(1-D)} - I_{L_{\mathrm{BB}}}\left(r_{L_{\mathrm{BB}}} + r_{D_2}\right) - v_{D_2} = V_{C_1}.\end{aligned} \tag{37}$$

Similarly, applying VSBC to L_{m} and deriving with (32) and (34) can obtain the representation of V_{C_2} as follows

$$\begin{aligned}&\left(V_{\mathrm{in}} + V_{C_1} - I_{L_{\mathrm{m}}} r_{L_1} - \left(I_{L_{\mathrm{m}}} + I_{L_{\mathrm{BB}}}\right) r_{ds}\right)\\ &\times \frac{D}{(1-D)} - I_{D_3}\left(r_{L_1} + r_{D_3}\right) - v_{D_3} = V_{C_2}.\end{aligned} \tag{38}$$

The voltage across L_{m} can be determined from the loop of either $N_1 - D_3 - C_2$ or $N_2 - D_4 - C_3$ during switch-off period. If from the loop of $N_2 - D_4 - C_3$, applying VSBC to inductor L_{m} and deriving with (32) and (35) can yield the following relationship

$$\begin{aligned}&\left(V_{\mathrm{in}} + V_{C_1} - I_{L_{\mathrm{m}}} r_{L_1} - \left(I_{L_{\mathrm{m}}} + I_{L_{\mathrm{BB}}}\right) r_{ds}\right)\\ &\frac{nD}{(1-D)} - I_{D_4}\left(r_{L_2} + r_{D_4}\right) - v_{D_4} = V_{C_3}.\end{aligned} \tag{39}$$

By substituting (37)–(39) into (1) and with simplifying, an expression of V_{o} is given as (see (40))

where the coefficients, A, B, and C, are defined as

$$A = (1+nD)^2 D, \tag{41}$$

$$B = (1+nD), \tag{42}$$

and

$$C = (1+n)^2 D, \tag{43}$$

respectively. In (36), the power loss of the converter includes

Table 3 Key parameters of the discussed example

Parameters	Values
V_{in} (input voltage)	40 V
V_{o} (output voltage)	400 V
P_{o} (output power)	200 W
R_{o}	800 Ω
r_{ds}	0.15 Ω
r_{D_1}, r_{D_2}, r_{D_3}, r_{D_4}	0.01 Ω
v_{D_1}, v_{D_2}, v_{D_3}, v_{D_4}	0.7 V
n (turns ratio)	3
$r_{L\mathrm{BB}}$	0.1 Ω
r_{L1}	0.2/0.35/0.5 Ω
r_{L2}	0.5 Ω

$$V_{\mathrm{o}} = \frac{\left[\frac{(1+nD)}{(1-D)^2} V_{\mathrm{in}} - \left(V_{D_1}\frac{D(1+nD)}{(1-D)^2} + V_{D_2}\frac{1+nD}{1-D} + V_{D_3} + V_{D_4}\right)\right]}{1 + \frac{A\cdot(1+n\cdot D)^2\cdot\left(r_{L_{\mathrm{BB}}} + r_{D_1} + r_{ds}\right)}{(1-D)^4 R_{\mathrm{o}}} + \frac{B^2\cdot\left(r_{L_{\mathrm{BB}}} + r_{D_2}\right)^2}{(1-D)^3 R_{\mathrm{o}}} + \frac{C\cdot\left(r_{L_1} + r_{ds}\right)}{(1-D)^2 R_{\mathrm{o}}} + \frac{r_{L_1} + r_{L_2} + r_{D_3} + r_{D_4}}{(1-D) R_{\mathrm{o}}}}, \tag{40}$$

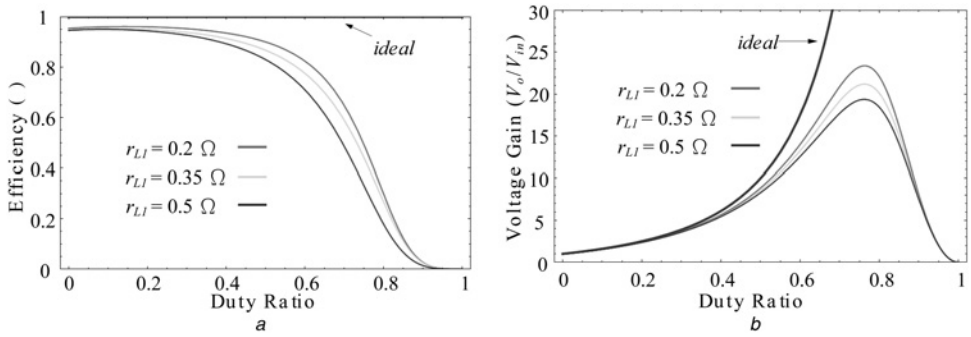

Fig. 6 *BBFIC in non-ideal condition*

a Relationship between efficiency and duty ratio
b Relationship between voltage gain and duty ratio

Table 4 Key parameters of the prototype

Parameters	Values
V_{in} (input voltage)	40 V
V_o (output voltage)	400 V
P_o (output power)	200 W
f_s (switch frequency)	50 kHz
duty ratio	0.5
C_1, C_2, C_3	100 μF
n (turns ratio)	3
L_{BB} (buck-boost inductance)	167 μH
L_m (magnetising inductance)	120 μH
L_{lk1} (leakage inductance)	1.2 μH

Table 5 Semiconductor devices in the prototype

Components	Type
SW (active switch)	FQP22N30
D_1 and D_2 (diodes)	SF1003G
D_3 (diode)	SF1005G
D_4 (diode)	BYV34-500

conduction loss $P_{\text{conduction\_loss}}$ and diode power consumption P_{diode}

$$P_{\text{loss}} = P_{\text{conduction\_loss}} + P_{\text{diode}}. \tag{44}$$

The $P_{\text{conduction\_loss}}$ and P_{diode} are computed as follows (see (45)) and

$$\begin{aligned} P_{\text{diode}} &= v_{D_1} i_{D_1} D + v_{D_2} I_{D_2}(1-D) \\ &\quad + v_{D_3} I_{D_3}(1-D) + v_{D_4} I_{D_4}(1-D). \end{aligned} \tag{46}$$

Substituting (40), (45), and (46) into (36) can find the representation of converter efficiency: (see (47))

An example is discussed for further understanding the efficiency performance of the proposed converter, in which key parameters are summarised in Table 3. Fig. 6*a* shows the curves of converter efficiency against duty ratio under various coupled-inductor resistances, which indicates that inductor resistance and duty ratio will influence efficiency significantly. A larger inductor resistance or a higher duty ratio will degrade voltage gain heavily, as shown in Fig. 6*b*. It can also be observed from Fig. 6*b* that the voltage gain is quite near the ideal curve while operating in low duty-ratio range. However, at a too large duty ratio, the voltage gain will diverge from the ideal and results in steep drop.

5 Experimental results

A prototype of the proposed converter is built to validate the feasibility of the converter, of which key parameters and semiconductor devices are listed in Tables 4 and 5, respectively. In the prototype, semiconductor devices will dominate circuit losses. Details of them are discussed in the followings. The power MOSFET, FQP22N30, is selected to serve as active switch for controlling current flow, of which maximum on-state resistance $R_{\text{DS(on)}}$ is 160 mΩ. SF1003G is employed as diodes D_1 and D_2, of which forward voltage is about 0.975 V and the reverse recovery time is 35 ns. The rectifier SF1005G is chosen as diode D_3; its forward voltage and reverse recovery time are 1.3 V and 35 ns, respectively. With regard to diode D_4, the ultrafast rectifier BYV34-500 is considered, which has 1.05 V forward voltage and 60 ns reverse recovery time. According to the design for inductive elements in Section 3.4, the inductances of L_{BB} and L_m for CCM operation at 100 W should be larger than 160 and 100 μH, respectively. In practical implementation, the L_{BB} and L_m are 167 and 120 μH, respectively. Fig. 7*a* shows the capacitor voltages, in which $V_{C_1} = 40$ V, $V_{C_2} = 80$ V, and $V_{C_3} = 240$ V. These magnitudes are in accordance with (2)–(4) as duty ratio is 0.5. Fig. 7*b* illustrates the voltage waveforms of diode 1 and diode 2, from which it can be seen that the voltage stresses of both diodes are the same and equal 80 V. Similarly, practical measurements of the voltages across diode 3 and active switch are shown in Fig. 7*c*.

$$\begin{aligned} P_{\text{conduction\_loss}} &= \left(\left(I_{L_{\text{BB}}}\right)^2\left(r_{L_{\text{BB}}} + r_{D_1} + r_{ds}\right) + \left(I_{L_m}\right)^2\left(r_{L_1} + r_{ds}\right)\right)D \\ &\quad + \left(\left(I_{L_{\text{BB}}}\right)^2\left(r_{L_{\text{BB}}} + r_{D_2}\right) + \left(I_{D_3}\right)^2\left(r_{D_3} + r_{L_1}\right) + \left(I_{D_4}\right)^2\left(r_{D_4} + r_{L_2}\right)\right)(1-D) \end{aligned} \tag{45}$$

$$\eta = \frac{\left[1 - \frac{1(1-D)^2}{V_{\text{in}}(1+nD)}\left(V_{D_1}\frac{D(1+nD)}{(1-D)^2} + V_{D_2}\frac{1+nD}{1-D} + V_{D_3} + V_{D_4}\right)\right]}{1 + \frac{A\cdot(1+n\cdot D)^2\cdot\left(r_{L_{\text{BB}}} + r_{D_1} + r_{ds}\right)}{(1-D)^4 R_o} + \frac{B^2\cdot\left(r_{L_{\text{BB}}} + r_{D2}\right)^2}{(1-D)^3 R_o} + \frac{C\cdot\left(r_{L_1} + r_{ds}\right)}{(1-D)^2 R_o} + \frac{r_{L_1} + r_{L_2} + r_{D_3} + r_{D_4}}{(1-D)R_o}} \tag{47}$$

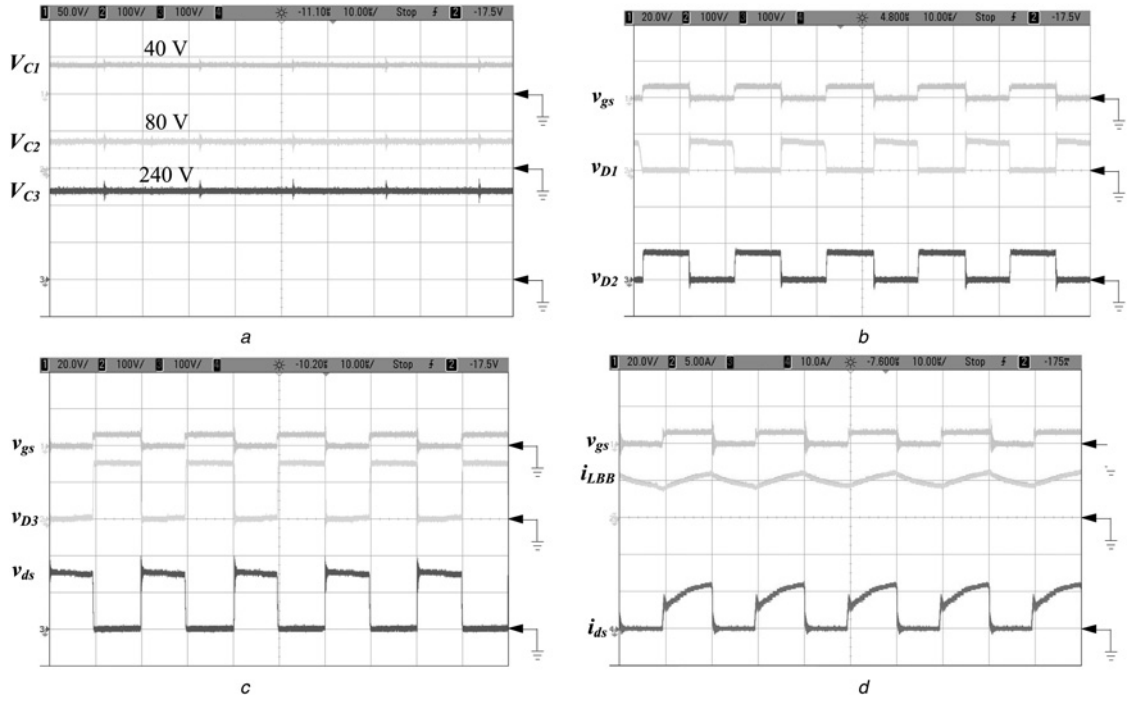

Fig. 7 *Experimental results of the proposed converter*

a Capacitor voltages of C_1, C_2, and C_3
b Voltage waveforms of diodes D_1 and D_2
c Voltage waveforms of diode D_3 and active switch
d Inductor current $i_{L_{BB}}$ and switch current i_{ds}
a (V_{C_1}: 50 V/div; V_{C_2} and V_{C_3}: 100 V/div; time: 10 µs/div) *b* (v_{gs}: 20 V/div; v_{D_1} and v_{D_2}: 100 V/div; time: 10 µs/div) *c* (v_{gs}: 20 V/div; V_{D_3} and v_{ds}: 100 V/div; time: 10 µs/div) *d* (v_{gs}: 20 V/div; $i_{L_{BB}}$: 5 A/div; i_{ds}: 10 A/div; time: 10 µs/div)

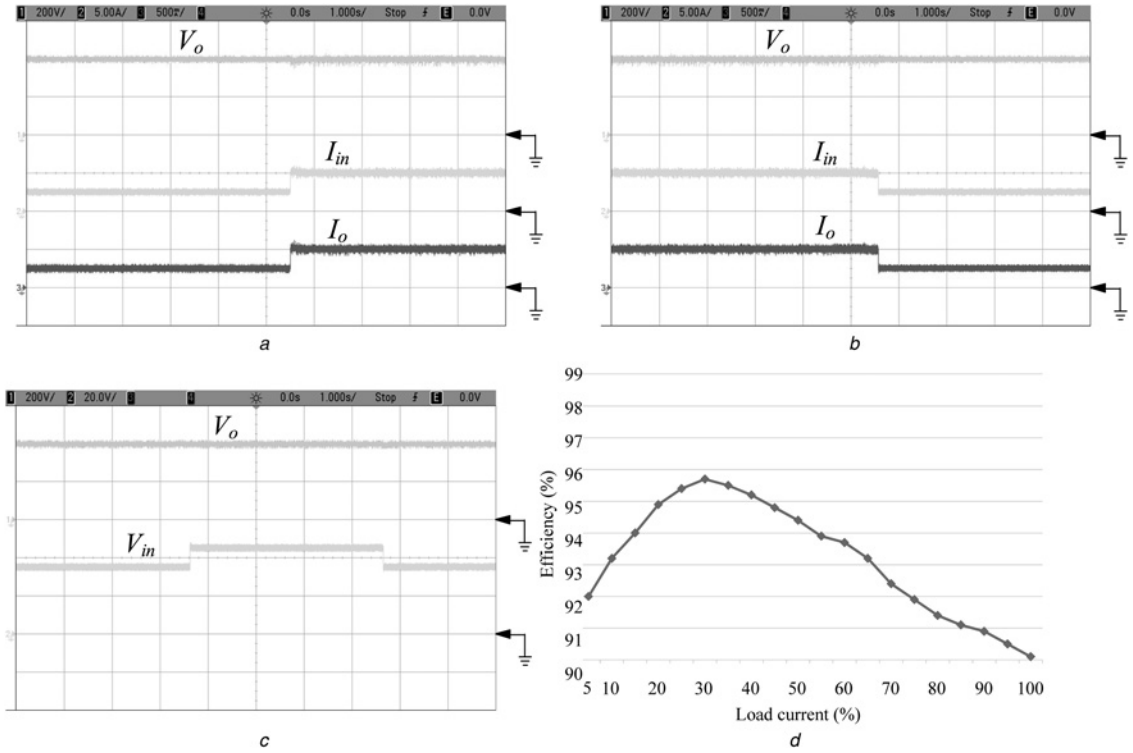

Fig. 8 *Converter performance illustration*

a Power change from half load to full load
b Power change from full load to half load
c Step change on input voltage under full load condition
d Measured efficiency
a (V_o: 200 V/div; I_{in}: 5 A/div; I_o: 500 mA/div; time: 1 s/div) *b* (V_o: 200 V/div; I_{in}: 5 A/div; I_o: 500 mA/div; time: 1 s/div)

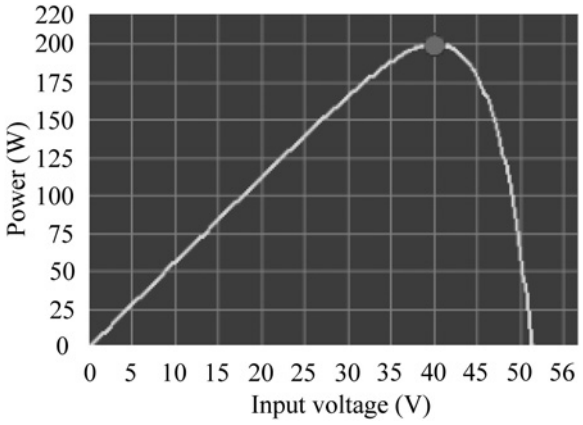

Fig. 9 *Illustration of the BBFIC processing PV panel with MPPT*

This figure depicts that diode 3 and active switch endure a voltage about 160 V, which is consistent with (8) or (12). Fig. 7*d* is the inductor current $i_{L_{BB}}$ and switch current i_{ds}, which demonstrates that inductor current increases/decreases linearly and the BBFIC operates in CCM under the inductance design in Section 3. Measured waveforms of output voltage, output current and input current, while power consumption from half load to full load and full load to half load, are presented in Figs. 8*a* and *b*, respectively. Figs. 8*a* and *b* reveal that the BBFIC is capable to providing constant output voltage and reaching rapid response even under a step change. Fig. 8*c* illustrates that while the input voltage changes instantaneously from 35 V to 45 V, the output voltage of the proposed high step-up converter can be regulated at 400 V within rapid transient response. Since the energy stored in the leakage inductor can be totally recycled, the maximum converter efficiency is up to 95.7%, as shown in Fig. 8*d*. Substituting the parameters in Table 3 into (47) can find that the theoretical efficiency at full load is 90.7%. From the hardware measurement in Fig. 8*d*, the practical efficiency is 90%, which is close to the estimated value. When BBFIC processes PV power and perturb-and-observe algorithm is adopted to complete maximum power point tracking, Fig. 9 shows the curve of power versus input voltage. Fig. 9 demonstrates that the proposed converter can draw maximum power from a PV panel.

6 Conclusions

In this paper, a novel single-switch DC/DC converter is proposed, which is able to boost a low input voltage to a much higher one. Therefore, the converter can be applied to PV panel or fuel cell power generation system. As compared with traditional high step-up converters, it is capable of providing high voltage gain without the use of excessive duty ratio or turns ratio. Furthermore, the energy stored in leakage inductor can be intrinsically recycled instead of additional clamp circuits, resulting in high conversion efficiency and simple circuit structure. A thorough theoretical analysis relating to voltage gain, voltage stress, current stress, and efficiency estimation is presented in this paper. A 200 W prototype is carried out to demonstrate the feasibility and correctness of the converter. Practical measurements have validated the converter and verified the analysis.

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